

Ultra-Low-Latency 10G TCP Endpoint

Description

Algo-Logic Systems' TCP Endpoint implements a full, reliable streaming network stack in FPGA logic. It allows applications in logic to be directly connected to Internet Protocol (IP) interfaces by opening, maintaining, and closing TCP Connections via Ethernet to other hardware or software endpoints.

The mature, reliable, and network-tested TCP Endpoint delivers high performance with ultra-low latency. It runs at the full 10 Gigabit Ethernet line rate with a clock speed synchronous with a MAC and application processing logic. It supports full duplex rates of 20 Gbps per instance. The implementation is portable between Intel and Xilinx FPGA devices and has been deployed on multiple platforms.

Algo-Logic's TCP Endpoint is available as a pre-integrated component in low latency applications or as a standalone IP. It has been deployed in customer applications including pre-trade risk-checks, complete tick-to-trade applications, and other flow processing applications. Algo-Logic provides in-house engineering support to ensure complete solution delivery with support for end-system and application-level fastest deployments.

Applications

- High frequency trading
- Tick-to-Trade systems
- Pre-trade risk checks
- Reliable, filtered feed redistribution
- Trading/arbitrage opportunity discovery
- Proprietary/algorithmic trading strategies
- Financial surveillance systems
- Network attached storage

Key Features and Use-Cases

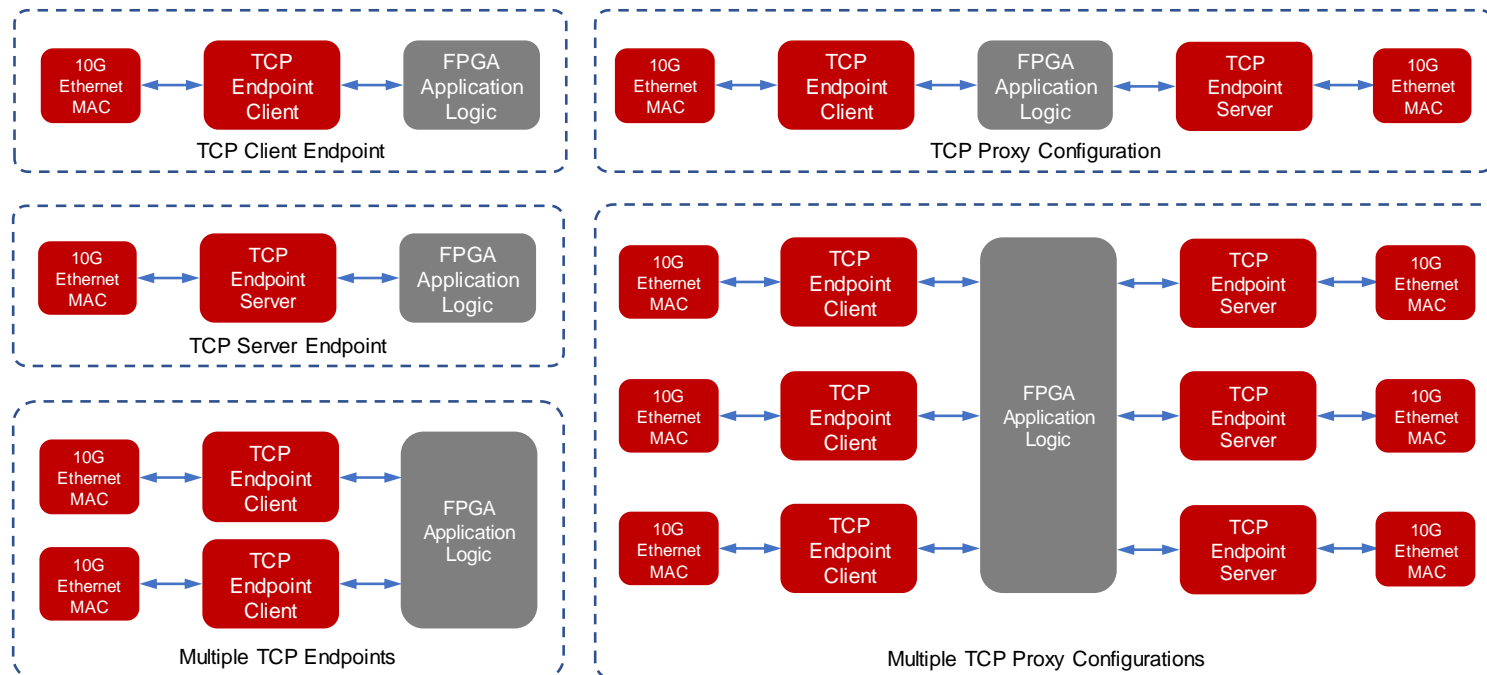
- Full TCP/IP stack in FPGA logic
 - Layer 1: IEEE802.3
 - Layer 2: IEEE802.3, ARP
 - Layer 3: IPv4 and ICMP
 - Layer 4: TCP
- Ultra-low latency
 - RTL design for optimal performance
 - Optional cut-through for receive (RX) and transmit (TX) data.
- Parameters
 - Retransmission timeouts
 - Size of shared on-chip retransmission buffer
 - Option for fast retransmission
 - Limits on retransmissions
 - TX Rewind
- Streaming Interfaces with in-order data
 - AXI-4
 - Avalon
- High network bandwidth
 - Multiple instances allow for more than 200 Gbps to a single FPGA device
- Control registers
 - Configurable over network or PCIe
- TCP option support: MSS, window scaling, timestamps
- Robust flow control and error control
- Advanced statistics for monitoring TCP sessions in real-time
- Exchange-certified in trading systems

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TCP Endpoint Metrics

Ultra-Low-Latency	32 nanoseconds@156.25 MHz (RX Latency from payload of packet to application)
Available # Sessions Per Instance	32, 64, 128, 256, 512, 4K, and 16K
Logic Footprint	~4% ALMs in Stratix V A7, ~1.5% CLB LUTs in Virtex UltraScale+ VU5P
US-Exchange-Certified	Yes
FPGA Devices Supported	Intel Stratix V, Intel Stratix 10, Xilinx Virtex Ultrascale+
Platforms Supported	Terasic DE5Net, ExaNIC V5P, Xilinx Alveo Series, Intel PAC D5005

TCP Endpoint Configurations



Ordering Codes

- Device: Intel Stratix V, Intel Stratix 10, Xilinx Virtex Ultrascale+
- Platforms: Terasic DE5Net, ExaNIC V5P, Xilinx Alveo Series, Intel PAC D5005
- Optional reference design compile-time parameters
 - Number of 10GE physical port instances
 - Client Endpoint, Server Endpoint, Proxy Configuration
 - Shared retransmission buffer size: e.g. 64KB, 128KB, 1024KB
 - Inquire for more options