

# Extensible Networking in Reconfigurable Hardware

Invited Talk at Georgia Tech's Center for  
Experimental Research in Computer Systems



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## Fundamental Changes

### • Existing (Old School) Internet Technologies

- Shortest hop routing
- Best effort packet delivery
- Bit transport service

#### – Current Technologies

- Microprocessors (slow)
- ASICs (static)

#### – Current Problems

- Network routers have static functionality
- Packet filtering rules manually deployed into firewalls
- Services manually deployed into network
- Network becomes unstable when attacked by Internet worms and DDoS outbreaks

### • Extensible Network (New School) Services

- Best path routing
- Guaranteed Quality of Service
- Application-Level services

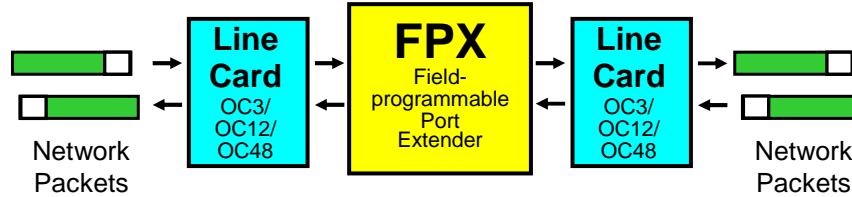
#### – New Technologies

- FPGAs
- Network Processors

#### – New Possibilities

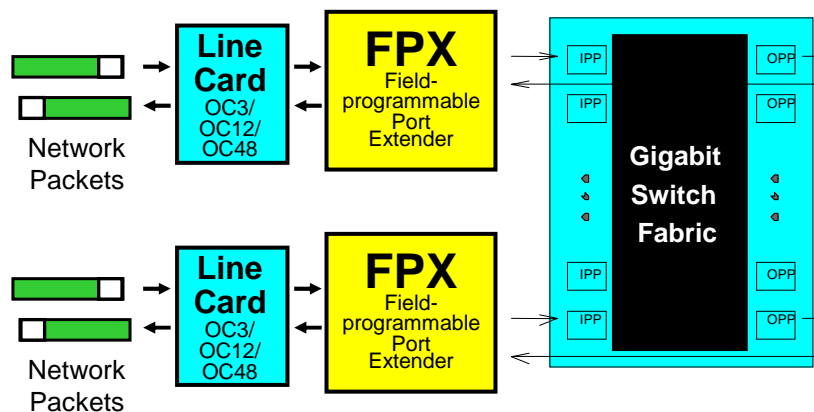
- Network routers with dynamic feature set
- Packet filtering rules automatically distributed to packet filtering nodes
- Services automatically deployed into network
- Robust for all possible traffic patterns

## Configuration of Network Packet Processor



- **Packet processing hardware performs:**
  - Packet classification
  - Packet forwarding
  - Address Translation
  - Data modification
  - Packet buffering
  - Active Networking (Application-level data processing)

## Configuration of Internet Router



- **Additionally, Router interface performs:**
  - Internet route lookup
  - Traffic policing and shaping

## Practical Platform for Extensible Hardware

- Suitable platform for shared development
  - Open platform
- Well-defined hardware interface
  - Suitable for System-on-Chip (SOC) Implementation
- Complete design methodology
  - Automatic flow from design to implementation
- Physical Implementation tools
  - Allow synthesis, place, and route with existing tools
- System management tools
  - Link static and dynamic functionality

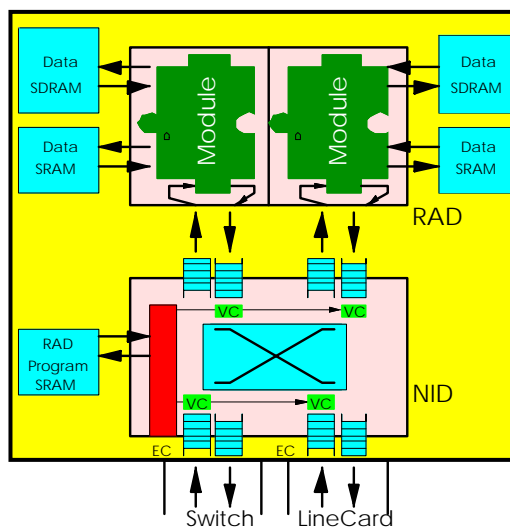
## Field Programmable Port Extender (FPX)

### • RAD

- Large Xilinx FPGA
- Attaches to SRAM and SDRAM
- Reprogrammable over network
- Provides two user-defined Module Interfaces

### • NID

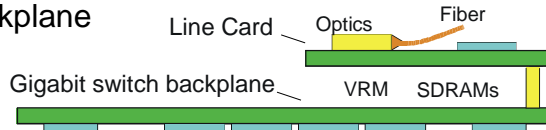
- Provides Utopia Interfaces between switch & line card
- Forwards cells to RAD
- Programs RAD



## Port Processing at edge of Gigabit Switch

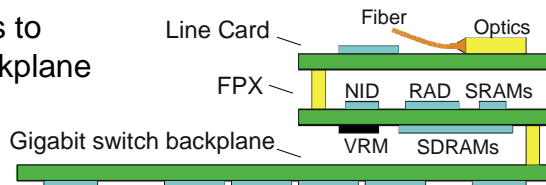
- **Original Network Switch**

- Line card connects to Gigabit switch backplane

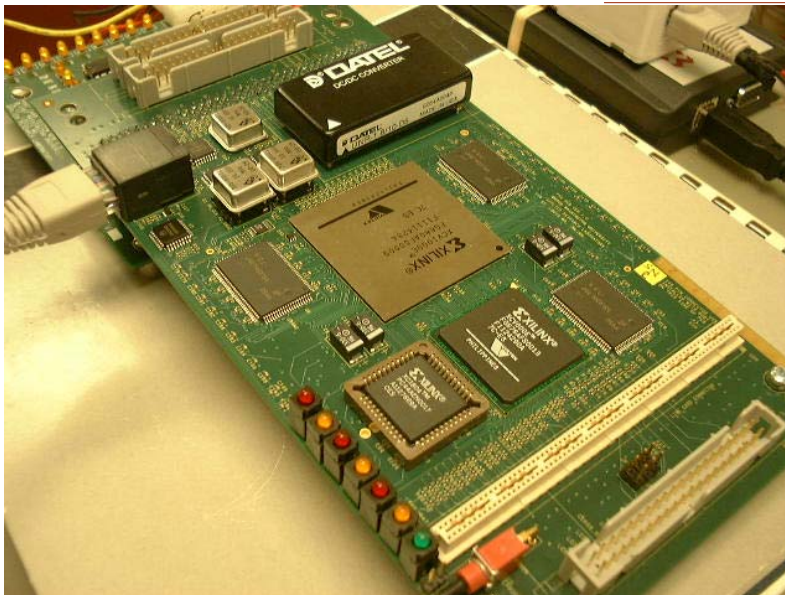


- **FPX-Enhanced Router**

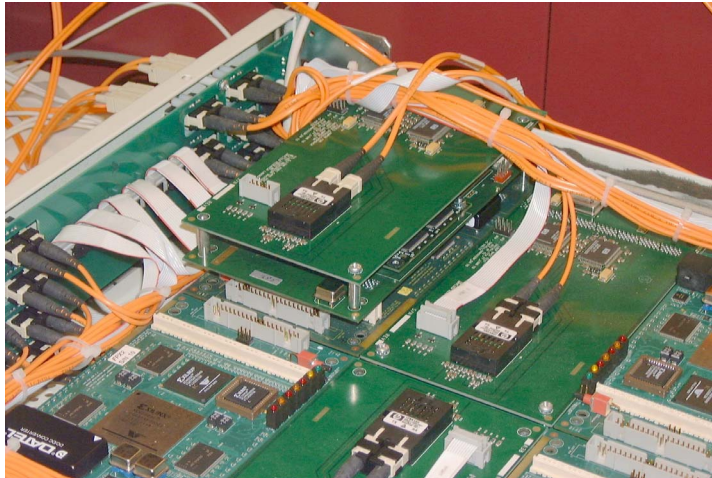
- Line card connects to Gigabit switch backplane



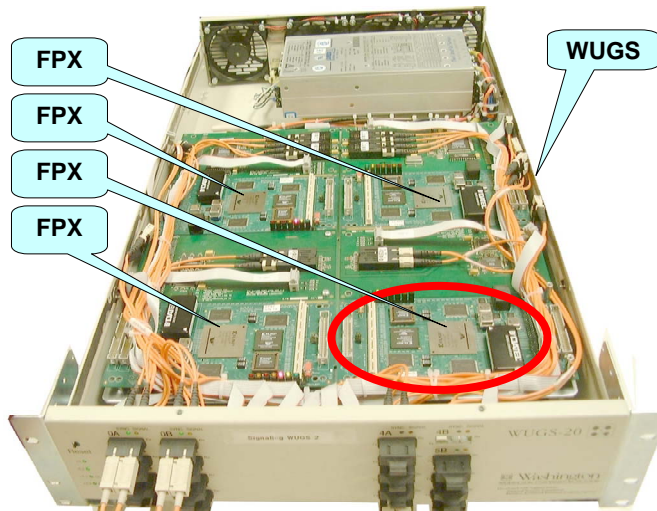
## Photograph of the FPX



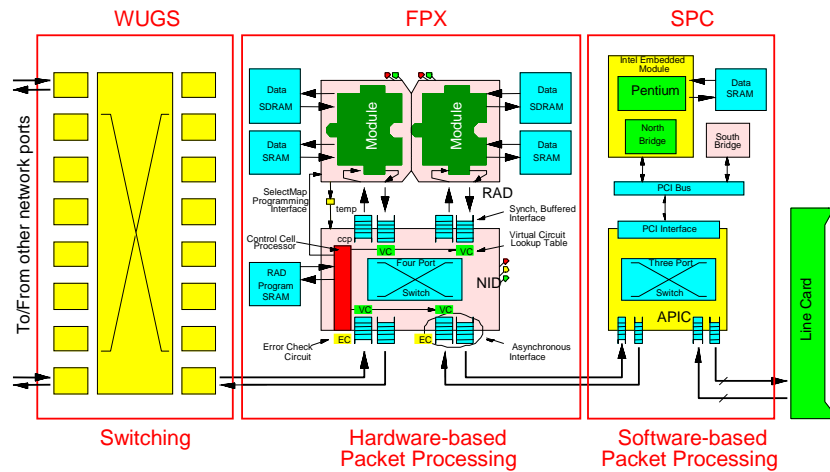
## Stacked FPX / SPC / Line card



## Washington University Gigabit Switch with FPX Devices



## Switch, FPGA, & Processor Configuration



## Applications for Extensible Networks :

### Network Security

## Dynamic Hardware Plugin contains:

- **Processing Module**

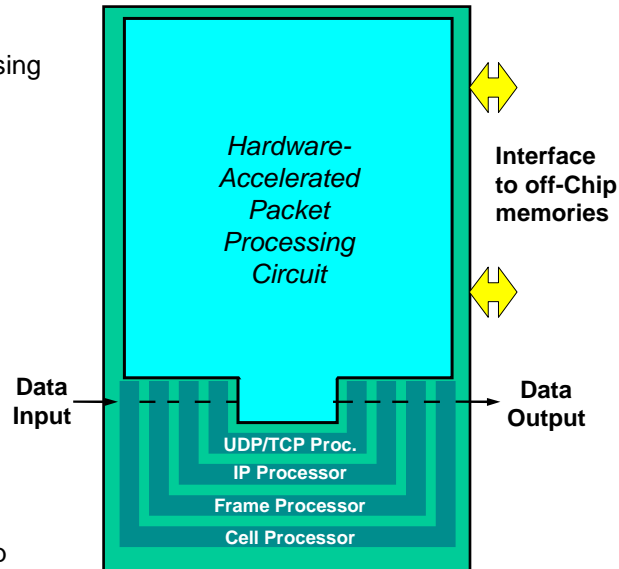
- Processes Data passing through the module

- **Protocol Wrappers**

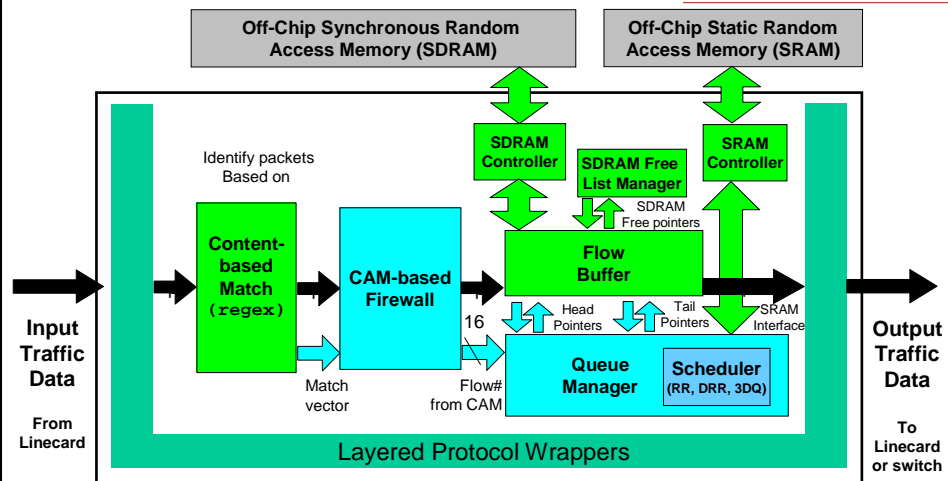
- Segment and reassemble Internet packets
- Compute packet headers, lengths, and checksums
- Provide reliable stream of data to processing module

- **Interfaces**

- Read and write packets to network
- Buffer data in off-ship SRAM and SDRAM



## Content-Aware Firewall on a Chip

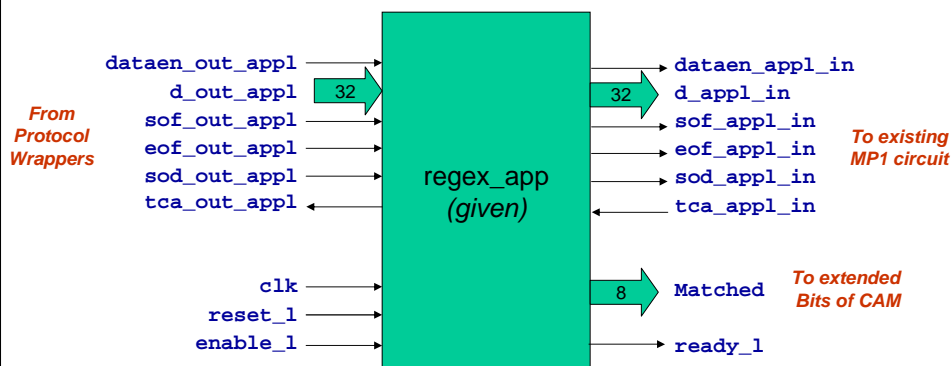


( Implemented on the RAD on the FPX, using a VirtexE 2000 FPGA )

## SPAM, Work, and Personal Phrase Lists

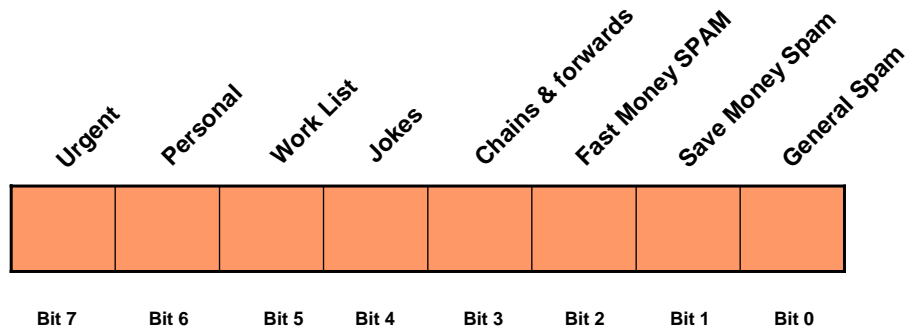
- **General Spam (Bit 0)**
    - “amazing”
    - “CALL NOW”
    - “Limited Time Offer”
  - **Save Money SPAM (Bit 1)**
    - “Consolidate”
    - “full refund”
  - **Fast Money SPAM (Bit 2)**
    - “MAKE MONEY FAST”
    - “Work from home”
  - **Chains and Forwards (Bit 3)**
    - “Read this”
    - “FWD”
  - **Jokes (Bit 4)**
    - “Joke”
    - “walks into bar”
  - **Work List (Bit 5)**
    - “Homework”
    - “Machine problem”
    - “CS536”
    - “Lockwood”
    - “Washington University”
  - **Personal List (Bit 6)**
    - “Mom”
    - “Dad”
    - “Call Home”
  - **Urgent (Bit 7)**
    - “Urgent”
    - “Emergency”
- Note: Underscored letters are case-insensitive*

## Content Matching Module



`wrapper_module.vhd`

## Content Match Vector



- Bit is set (1) if any phrase in a category is found anywhere in payload
- Bit is clear (0) if none of the phrases in the category appear in the payload

## Sample Content Match Vector

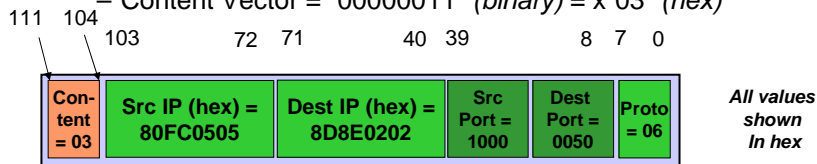


- “Consolidate your loans. CALL NOW”

## Packet matching w/ Content Addressable Memory

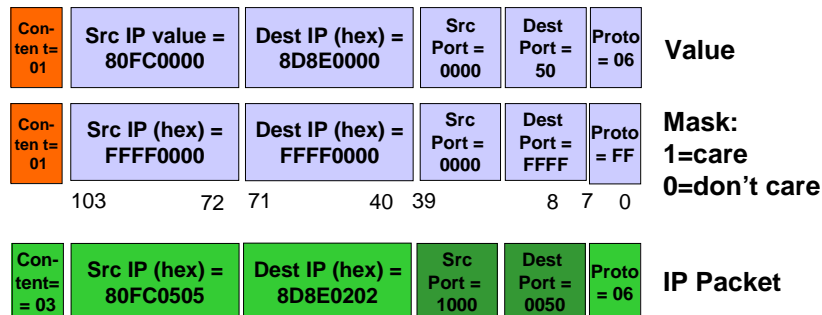
### • Sample Packet:

- Source Address = 128.252.5.5 (*dotted.decimal*)
- Destination Address = 141.142.2.2 (*dotted.decimal*)
- Source Port = 4096 (*decimal*)
- Destination Port = 80 (*decimal*)
- Protocol = TCP (6)
- Payload = "Consolidate your loans. CALL NOW"
  - Payload Lists = { General SPAM (0), Save Money SPAM (1) }
  - Content Vector = "00000011" (*binary*) = x"03" (*hex*)



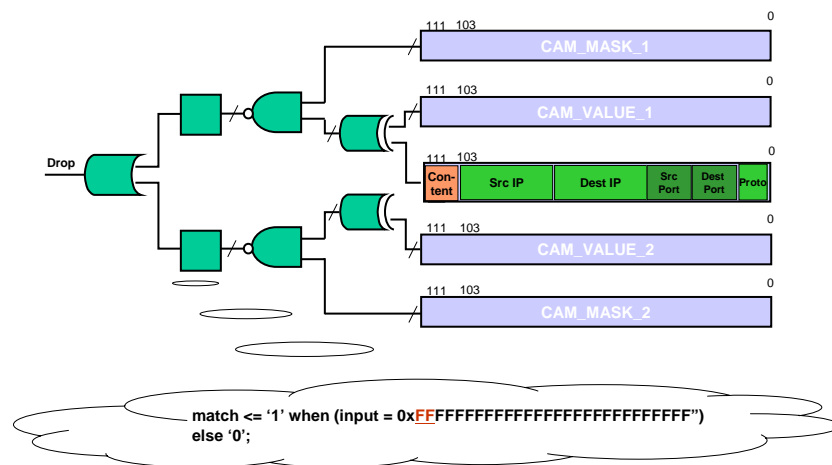
## Sample Filter

- Source Address = 128.252.0.0 / 16
- Destination Address = 141.142.0.0 / 16
- Source Port = Don't Care
- Destination Port = 80
- Protocol = TCP (6)
- Payload includes general SPAM (List 0)



**DROP the packet : It matches the filter**

## Basic Packet Classification Hardware



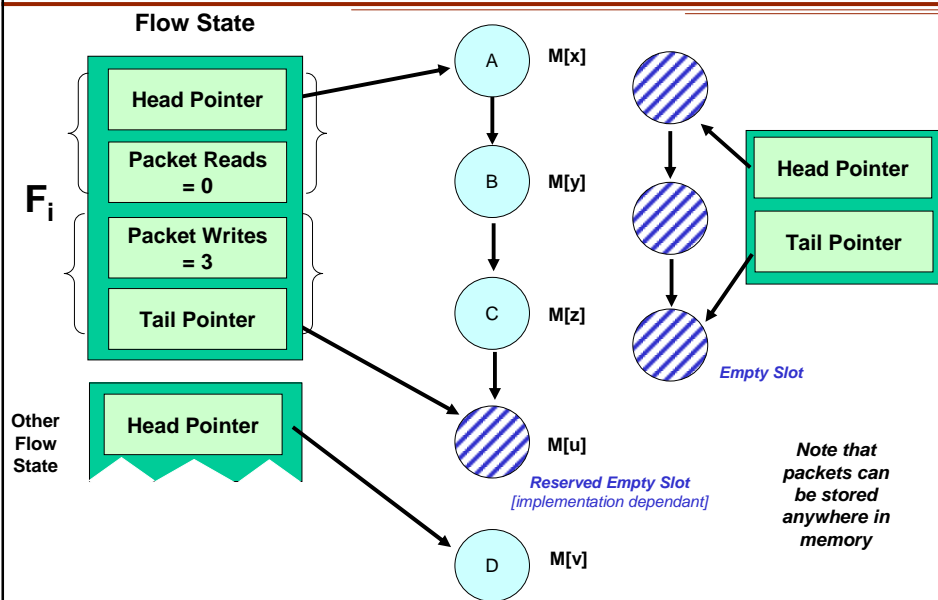
## Quality of Service

- **Gives some flows better service than others**
  - Zero-sum game :
    - The amount of bandwidth on a link is fixed.
  - Design the system to maximize reward
    - Not all Internet users are created equal.
    - Will users pay for something that is not well defined?
  - Some flows get worse service!
- **Applications**
  - Determine which flows to drop under heavy load
  - Try to provide virtual link with end-to-end guarantee on bandwidth and delay

## Data Queuing Outline

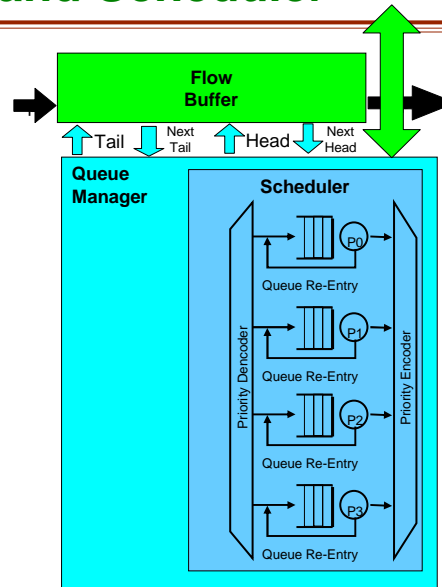
- **Types of Queuing**
  - Class-based
    - Priority-based Service Disciplines
    - Differentiated Services
  - Per-Flow
    - Fluid Fair Queuing / Weighted Fair Queuing
    - Constant-Time Queue Service Disciplines
  
- **Hardware Implementation of Flow Queues**
  - Running time limitations in Gigabit networks

## Queue Management

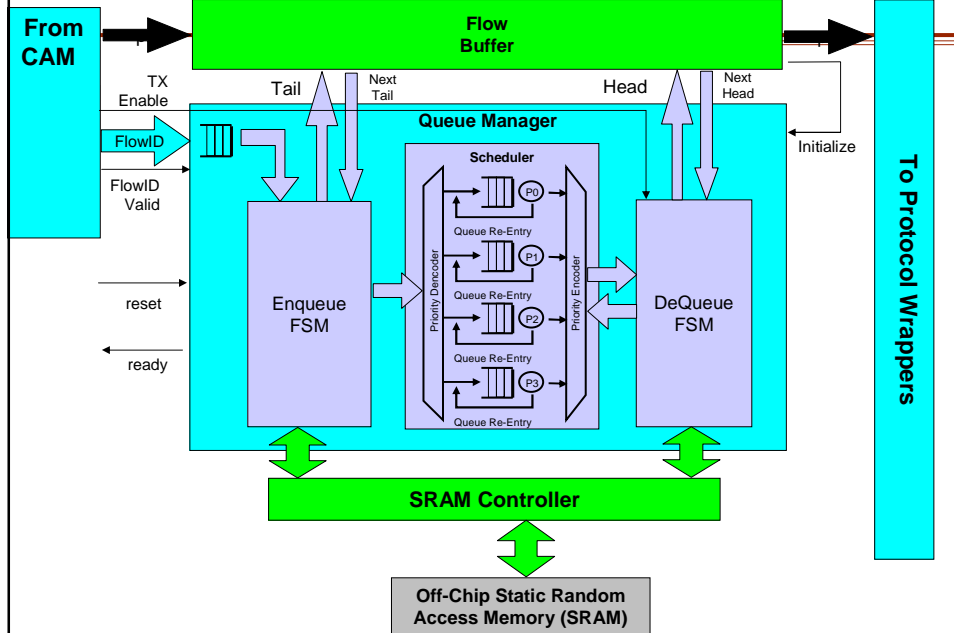


# Queue Manager and Scheduler

- The 3DQ Scheduler for MP3 combines priority-based scheduling with flow-based scheduling
  - Supports four priority levels
    - Each implemented as a CoreGen FIFO that stores Flow IDs
  - Supports per-flow queuing
    - Backlogged flows are serviced in a round-robin manner



# Detail of Queue Manager & Scheduler



## Extensible Interface to Flow Buffer

--Interface with the Queue Context

-- From the Queue Manager

```
Tail: in std_logic_vector(31 downto 0);
TailValid: in std_logic;
```

-- To the Queue Manager

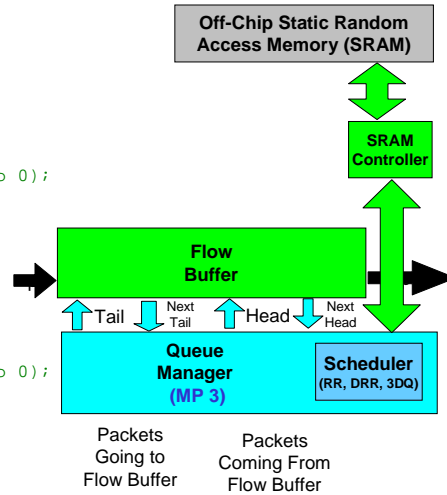
```
NextTail: out std_logic_vector(31 downto 0);
NextTailValid: out std_logic;
```

-- From the Queue Manager

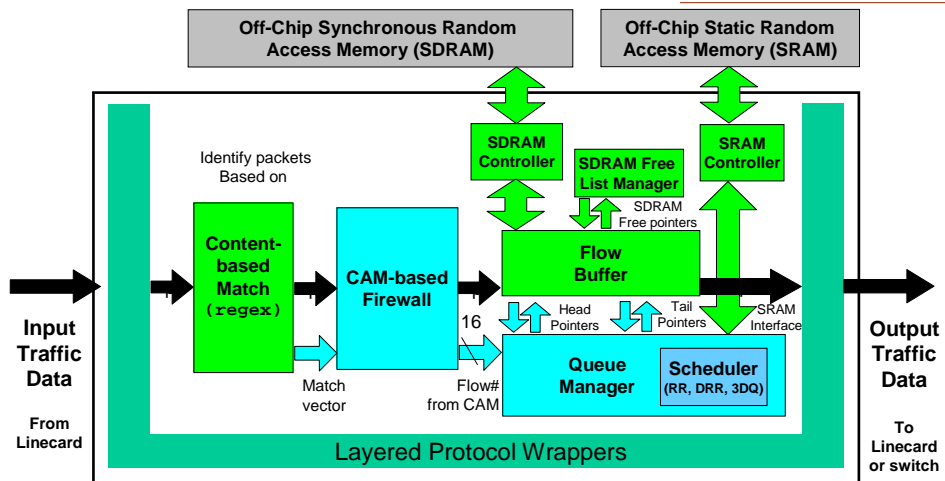
```
Head: in std_logic_vector(31 downto 0);
HeadValid: in std_logic;
```

-- To the Queue Manager

```
NextHead: out std_logic_vector(31 downto 0);
NextHeadValid: out std_logic;
```

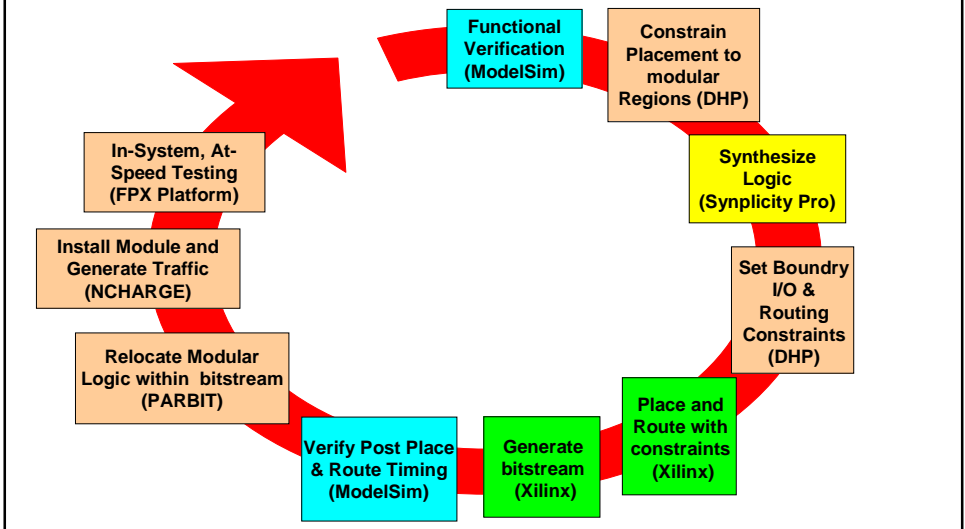


## Content-Aware Firewall on a Chip

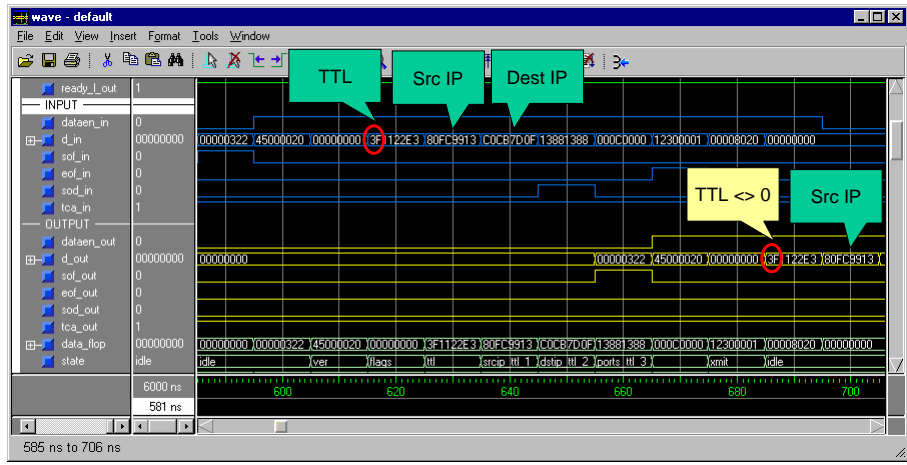


( Implemented on the RAD on the FPX, using a VirtexE 2000 FPGA )

# DHP Design Flow



# Packet Processing Waveform



## Synthesizing the Design (Synplicity)

Listing of the synthesizable vhd files in the design. The files are listed in **bottom-up** order

Target FPGA  
Xilinx Virtex-E XCV2000E -7 FG680

31 - Lockwood - Applied Research Laboratory -- Extensible Networking

Washington University in St. Louis

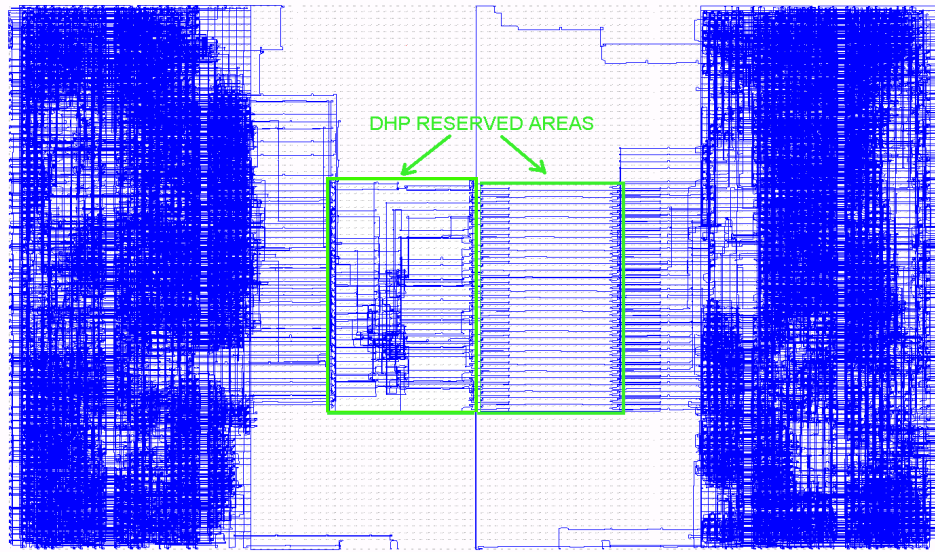
## DHP Implementation on the FPX

- **Programming Module onto the Reprogrammable Application Device (RAD)**
  - Circuit on XCV2000E
  - SRAM and SDRAM Interfaces
  - Control Cell Processor
  - Holds 2+ DHP Modules
  - Reprogrammable over network

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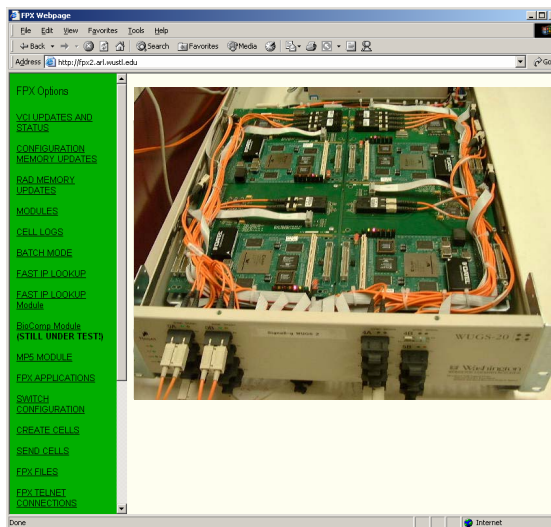
Washington University in St. Louis

## Floorplannings - INFRA



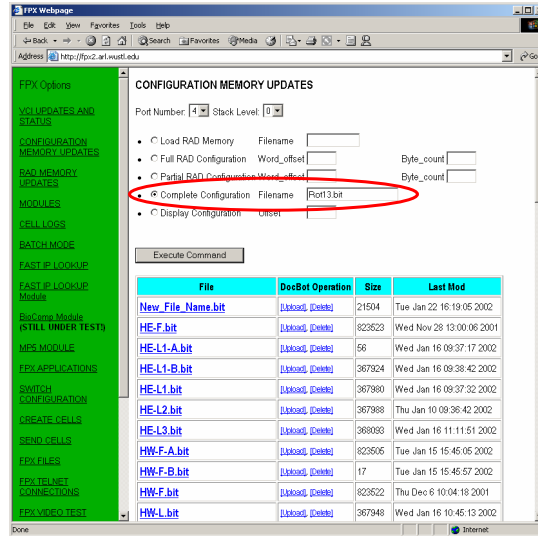
## NCHARGE Homepage

- **Web interface to communicate with the FPX**
- **Menu Functions**
  - Route traffic flows
  - Reprogram hardware
  - Upload bitfiles
  - Read & write on-chip Memory
  - Create test cells

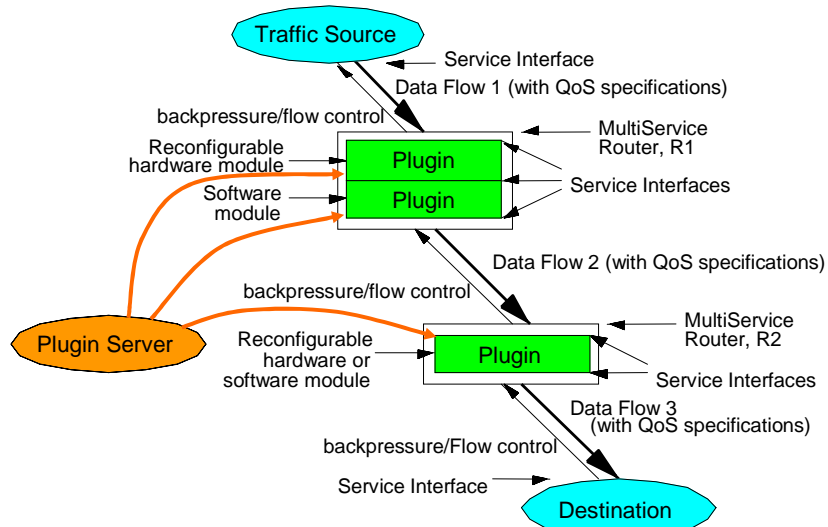


## GUI to Install New Hardware Module

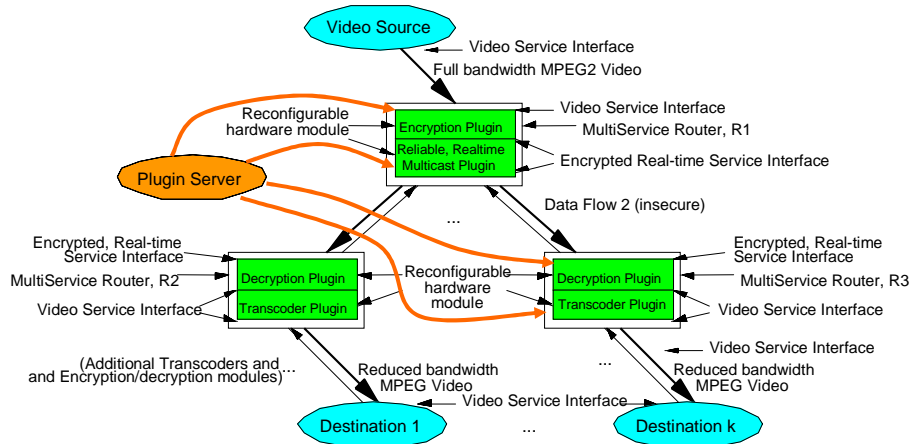
- Allows uploading and downloading of full or partial bitfiles
- Allows user to select a bitfile for programming
- FPGA reconfigures when user presses 'Execute Command'



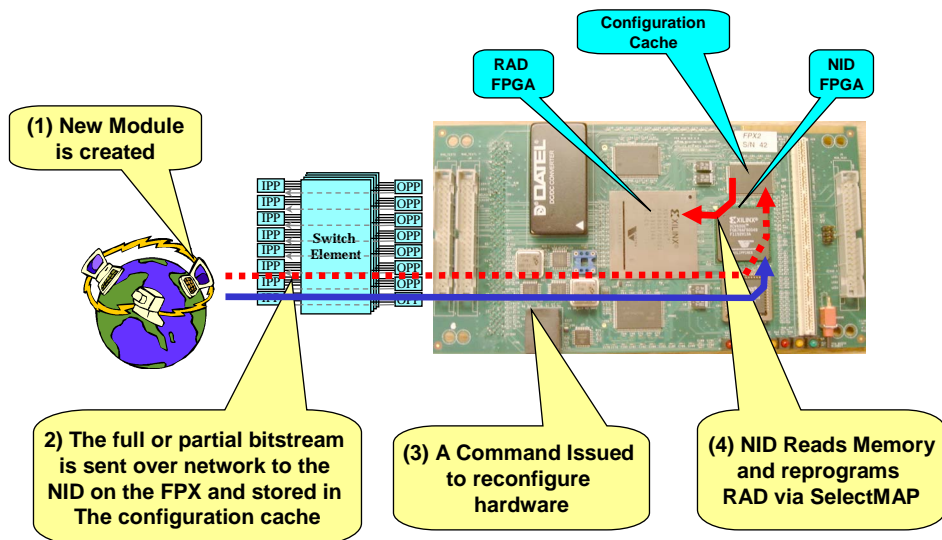
## Hardware Plugin Service Model



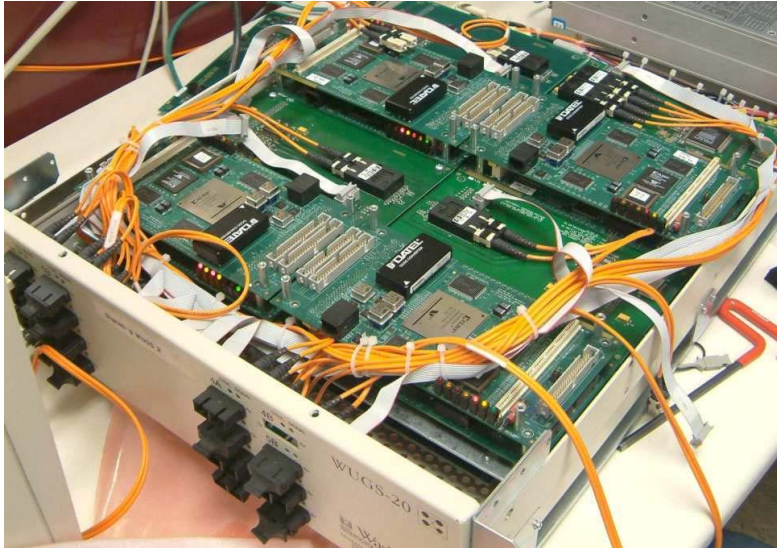
## Example: Secure, Reliable, Video Distribution



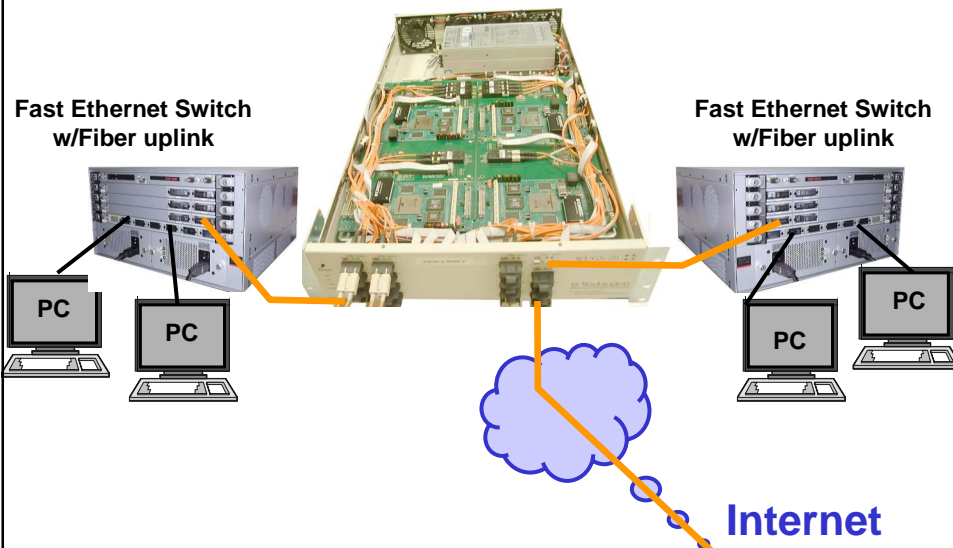
## Reprogramming the FPX



## Simultaneous Programming Within a Switch



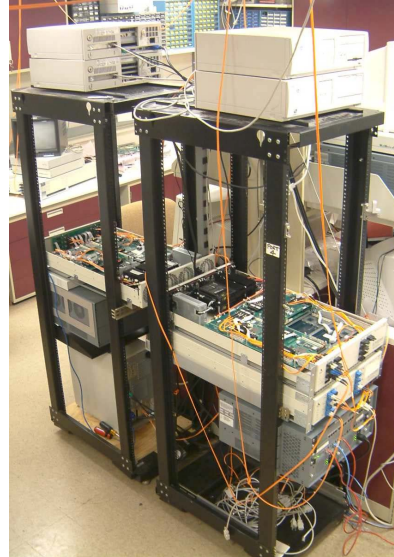
## Interfacing with Computers & Internet



## FPX Platform platform developed



**FPX combined with WUGS  
to route and process  
Internet packets**



## Other Modules Implemented

- **IPv6 Tunneling Module**
  - Tunnels IPv6 over IPv4
- **Statistics Module**
  - Event counter
- **Traffic Generator**
  - Per-flow mixing
- **Video Recoder**
  - Motion JPEG
- **Embedded Processor**
  - KCPSM
- **IPv4 CAM Filter**
  - 104 Bit header matching
- **Fast IP Lookup (FIPL)**
  - Longest Prefix Match
  - MAE-West at 10M pkts/second
- **Packet Content Scanner**
  - Reg. Expression Search
- **Data Queueing**
  - Per-flow queue in SDRAM

## Summary

- **Extensible Network Technology**
  - Provides high degree of configurability
  - Provides high performance
- **Field Programmable Port Extender (FPX) Platform**
  - Well-defined Application Programming Interface
  - Web interface simplifies FPX control and configuration
  - 85 FPX devices built
  - Over 30 Hardware applications developed & tested on FPX
- **Applications**
  - Internet Protocol (IP) Protocol Processing
  - Network Security (Firewall)
  - Quality of Service (Flow Scheduler)
  - Multi-video processing Platform
  - Your modules!

## FPX used for Hands-on Tutorials

Gigabit Kits workshops with FPX Tutorials held 1/01, 8/01, 1/02, & 6/02



Participants Programmed FPX Modules in the CAD Laboratory



Then tested modules in lab



- [June 2002 FPX Workshop](#) John W Lockwood, Todd Sproull, James Moscola, David Schuehler, Dave Lim, Sarang Dharmapurikar, Chris Neely, *Gigabit Kits Workshop*, Saint Louis, MO, June 19-20, 2002.
- [January 2002 FPX Workshop](#) John W Lockwood, David Taylor, James Moscola, Todd Sproull, Dave Lim, *Gigabit Kits Workshop*, Saint Louis, MO, January 3-4, 2002.
- [August 2001 FPX Workshop](#) John W Lockwood, Henry Fu, Todd Sproull, Sarang Dharmapurikar, Edson Horta, Dave Lim *Gigabit Kits Workshop*, Saint Louis, MO, August 15-16, 2001.
- [January 2001 FPX Workshop](#) John W Lockwood, David E. Taylor, Todd Sproull, Sarang Dharmapurikar, Florian Braun. *Gigabit Kits Workshop*, Saint Louis, MO, January 11-12, 2001.

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      - David Lim
      - James Moscola
      - David Schuehler
      - Chris Neely
      - Chris Zuver
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