ALGORITHMS IN LOGIC

HTTP://ALGO-LOGIC.COM

Algorithms in Logic for Ultra Low Latency Networking

Full-stack applications in Field Programmable Gate Arrays (FPGAs)

John W. Lockwood, PhD, CEO, Algo-Logic Systems, Inc.

Hot Interconnects: Aug 19, 2021

ALGO-LOGIC

Quick Outline

- Algo-Logic Systems, Inc.
  - Who we are
  - Products and Solutions
  - Applications and Customers

- **Algorithms in FPGA Logic**
  - Accelerated Trading
    - Tick to Trade, Pre-Trade Risk Checks, and Exchange Building Blocks
  - Key Value Store (KVS)
  - Packet Classification using HLS

- **Development Frameworks on off-the-shelf partner SmartNIC/DPU/FPGA Platforms**
  - Intel PAC
  - Cisco Nexus V5P/V9P
  - Xilinx ALVEO

About Algo-Logic Systems Inc

- Algo-Logic Systems, Inc
  - Maps Algorithms into Logic
  - Established in 2009 and remains a privately-held C-Corporation
    - Motivated to productize Fintech products by HB, Raj, and Andy Bach of NYSE
  - Based in Silicon Valley (San Jose, CA)

ALGORITHMS IN LOGIC

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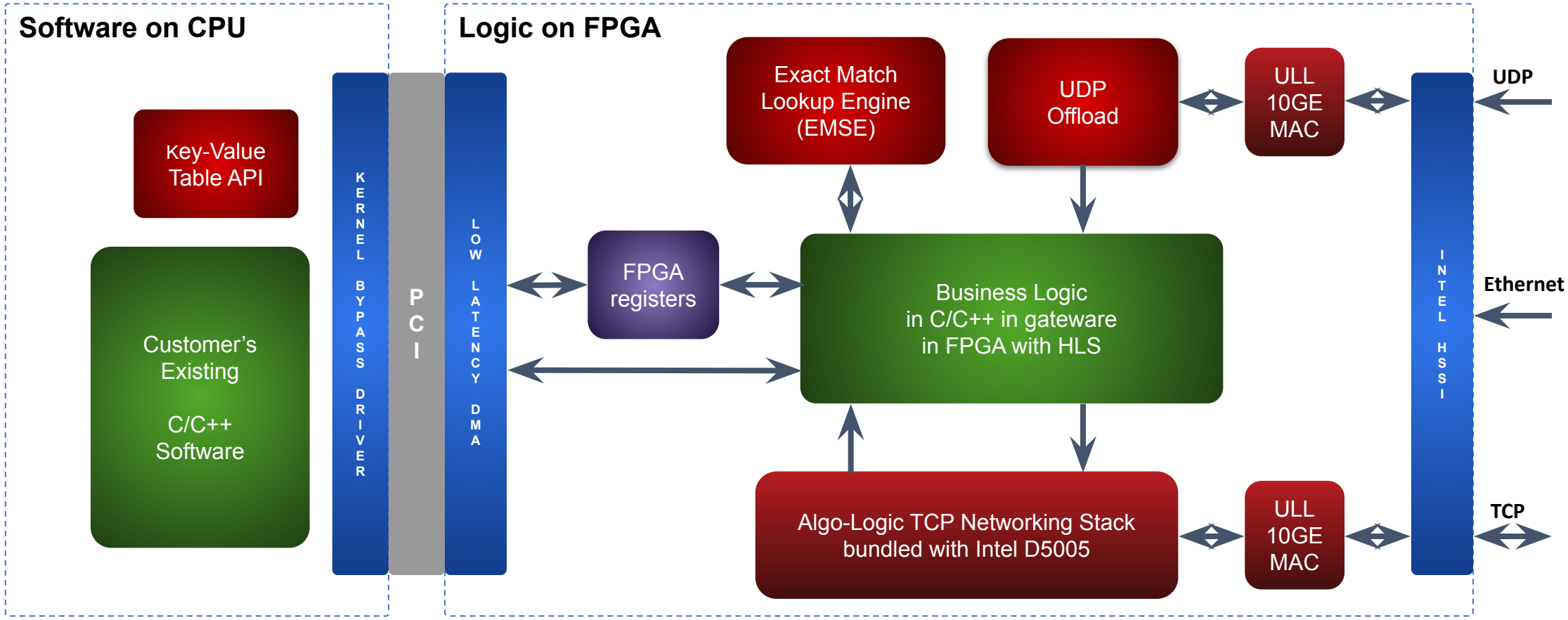
- **Products and Solutions**
  - FPGA IP Cores for Ultra-Low-Latency (ULL) networking
    - MAC, TCP, UDP, EMSE
  - Complete FPGA Solutions in FPGA logic
    - for Accelerated Finance and Real-Time Data
  - Full Stack Development Frameworks to trade on multiple exchanges

Nasdaq CME Group

- **Customers Include:**
  - Multinational Banks, Proprietary Trading Firms, and Stock Exchanges
  - Datacenter equipment providers
  - Real-Time Data providers

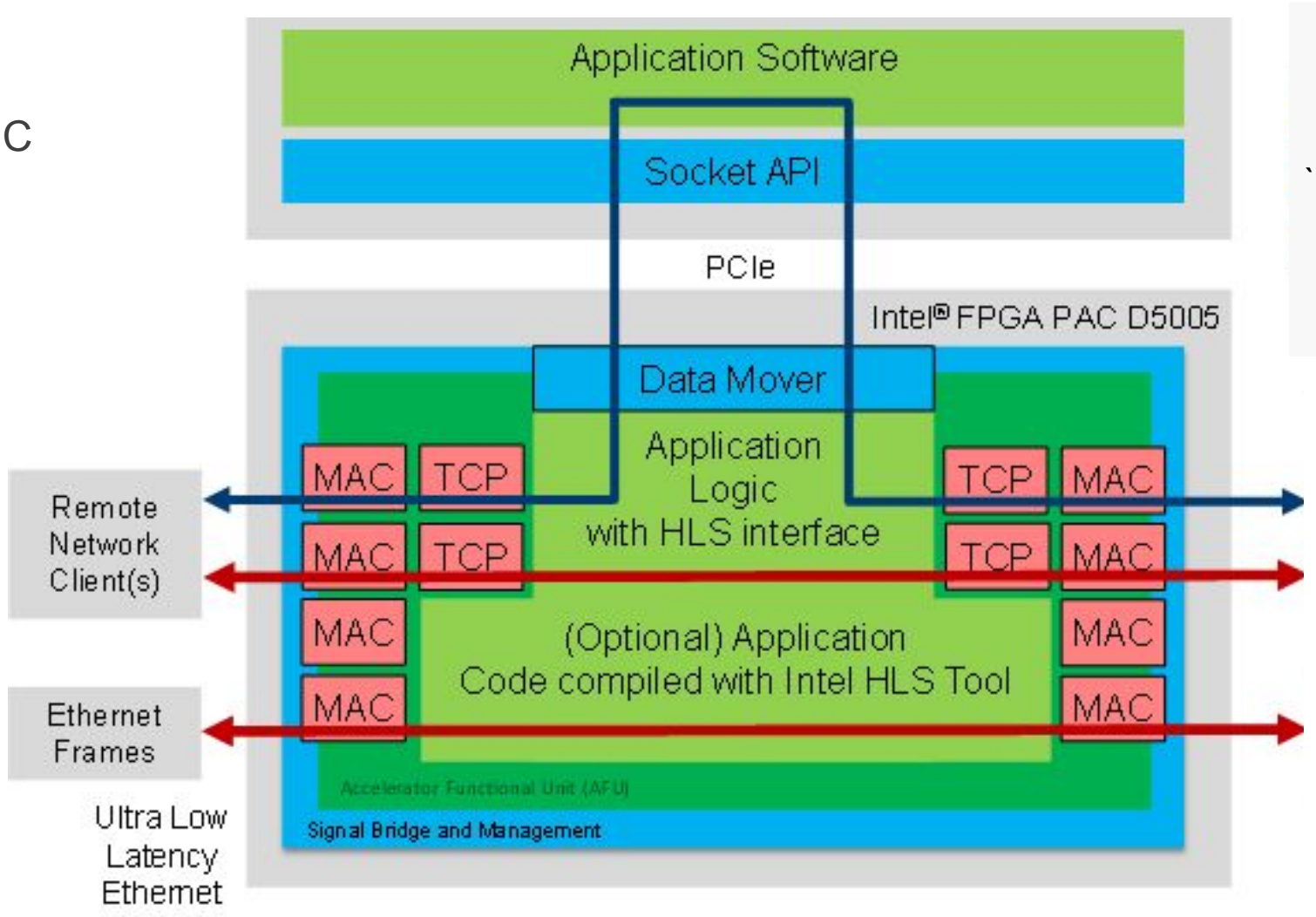
Algo-Logic's FPGA / SmartNIC Development Framework



Algo-Logic IP Cores
Card Vendor Hardware + Software Driver
Customer Software and Business Logic

FPGA Cards are Ideal Solution for Ultra Low Latency Networking

- **FPGA Platform**
  - PCIe card with FPGA
  - Fast Data Mover / kernel-bypass NIC
  - High Level Synthesis (HLS)
- **Algo-Logic Provides**
  - Ultra-Low Latency MACs
  - UDP/TCP Endpoints in Logic
  - Cut-through data processing
  - APIs for C/C++ software apps
- **Ideal Solution for**
  - High-speed Trading
  - Pre-Trade Risk Checks
  - Trading Gateways



Round-Trip Application Latency

Other 3rd party NIC

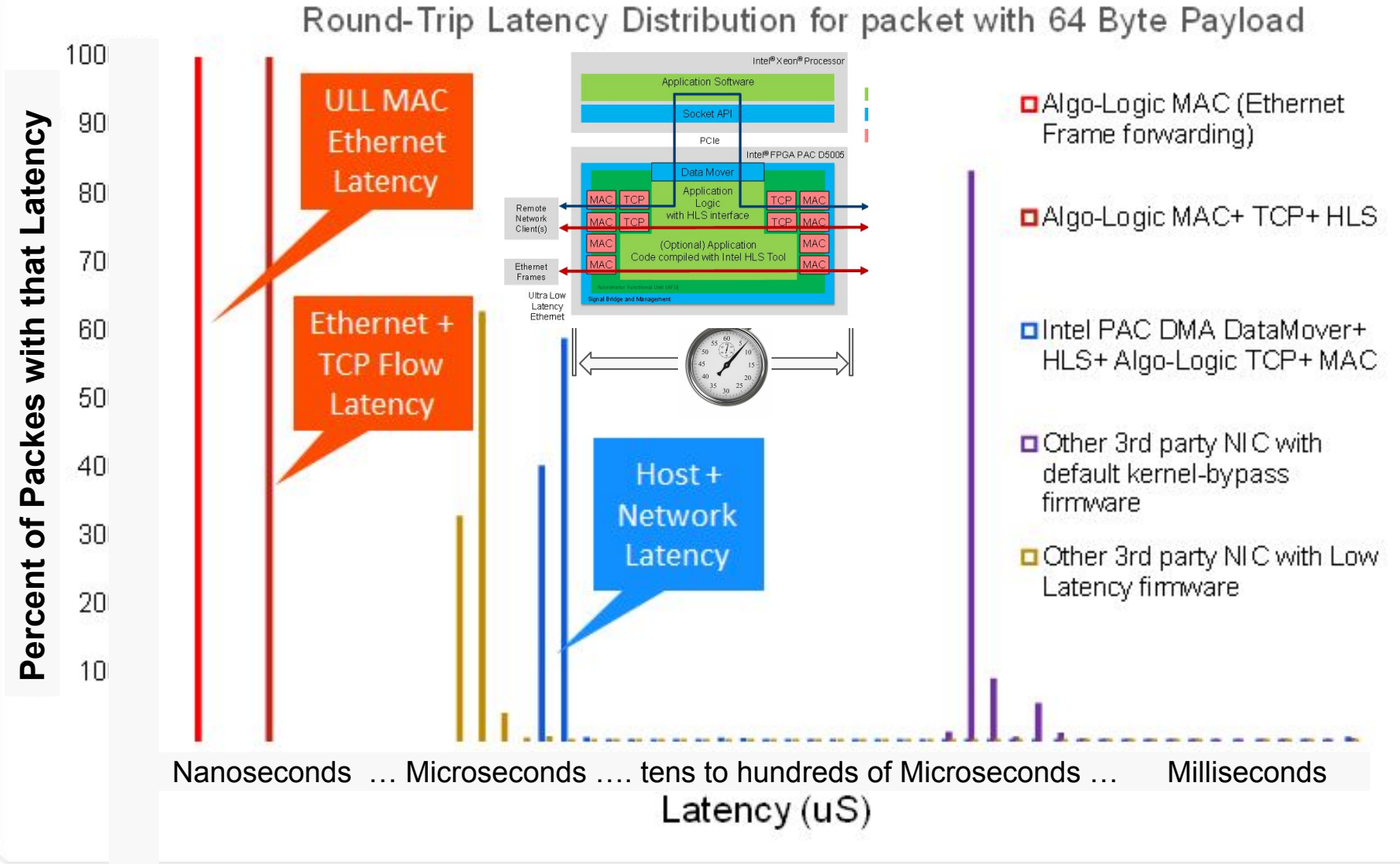
- Kernel Bypass
- Default Firmware
- Low Latency Firmware

This Host+Network

- Software API
- Intel Data Mover
- Algo-Logic MAC+TCP

Algo-Logic FPGA Logic

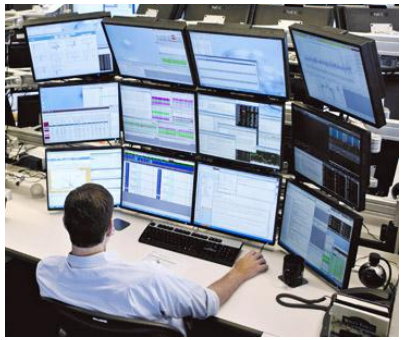
- ULL MAC, UDP, TCP
- Cut-through processing
- Deterministic latency
- HLS Interface for algorithms in logic coded in C/C++



Evolution of Trading Systems

- **From Specialists (humans) in a pit**
  - Trade on behalf of clients
  - Make markets by open outcry
  - Trade in minutes to seconds

- **To Trading with Software**
  - Automated trading using software from the desktop
  - Trade in seconds to milliseconds



- **To Co-located Hyper-optimized Datacenters**
  - Bypass the operating system kernel
  - Run in servers at co-location datacenters
  - Trade in milliseconds to microseconds

- **To FPGA-Accelerated**
  - Implement algorithms in logic to offload application to logic
  - Run on Field Programmable Gate Arrays (FPGA)
  - Trade in nanoseconds (< 0.000001 seconds)

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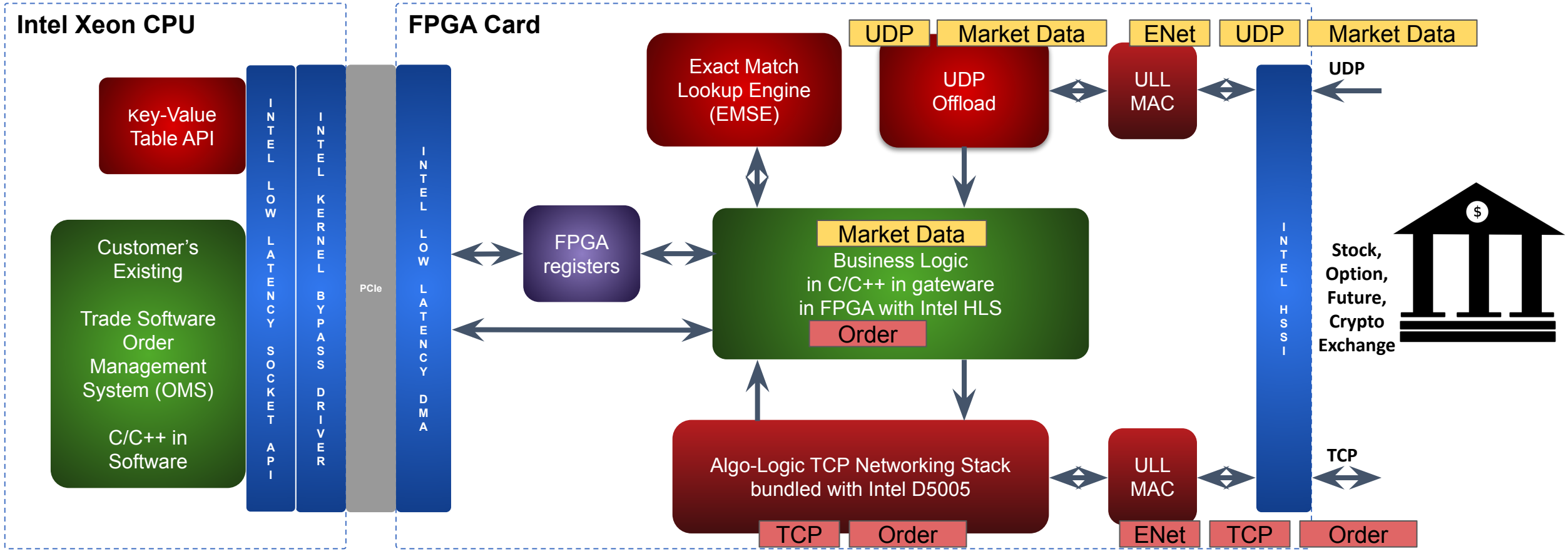
Algo-Logic Framework for FPGA-Accelerated Trading



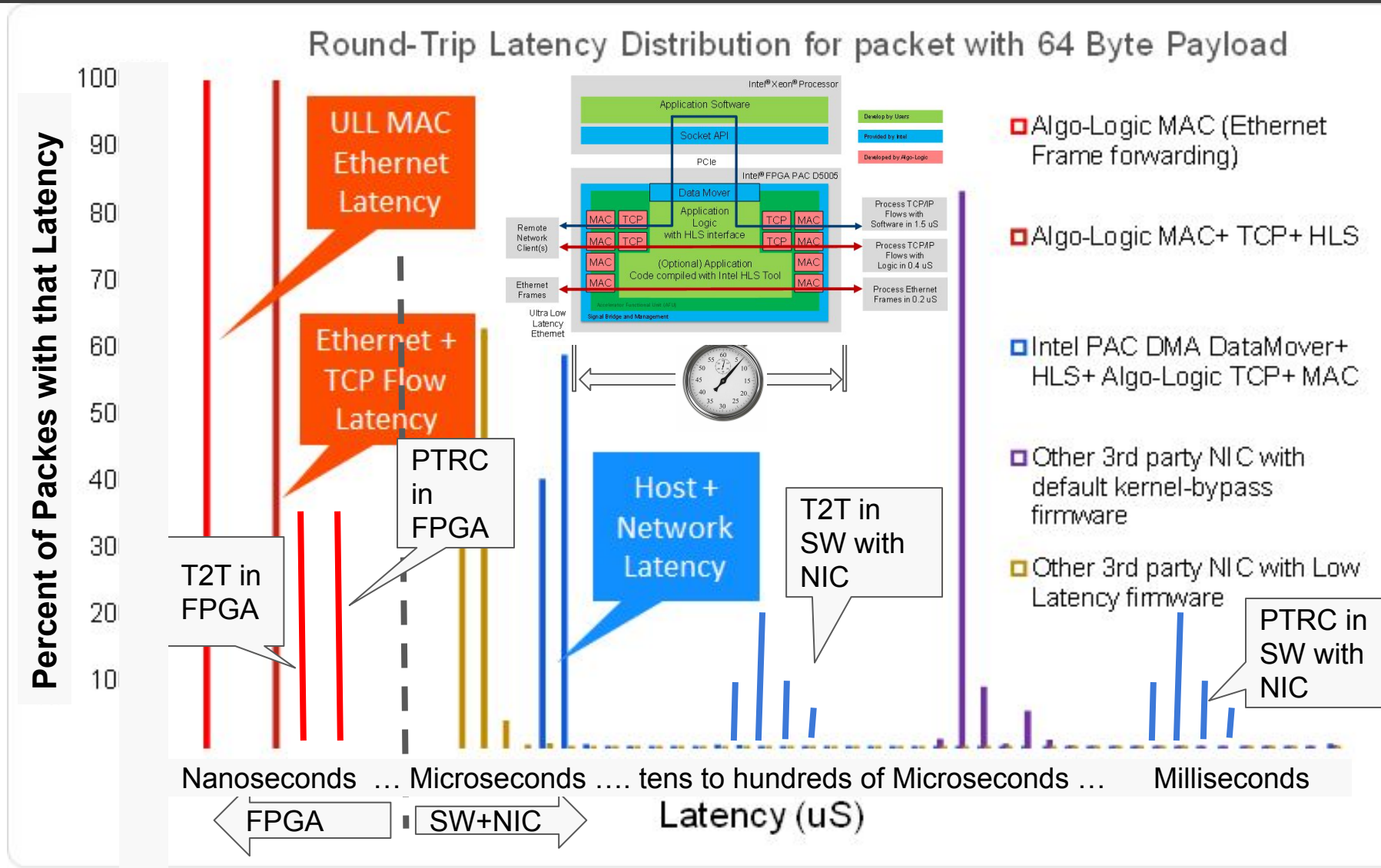
Algo-Logic IP Cores
Intel Hardware + Software Driver
Customer Software and Business Logic

Round-Trip Application Latency

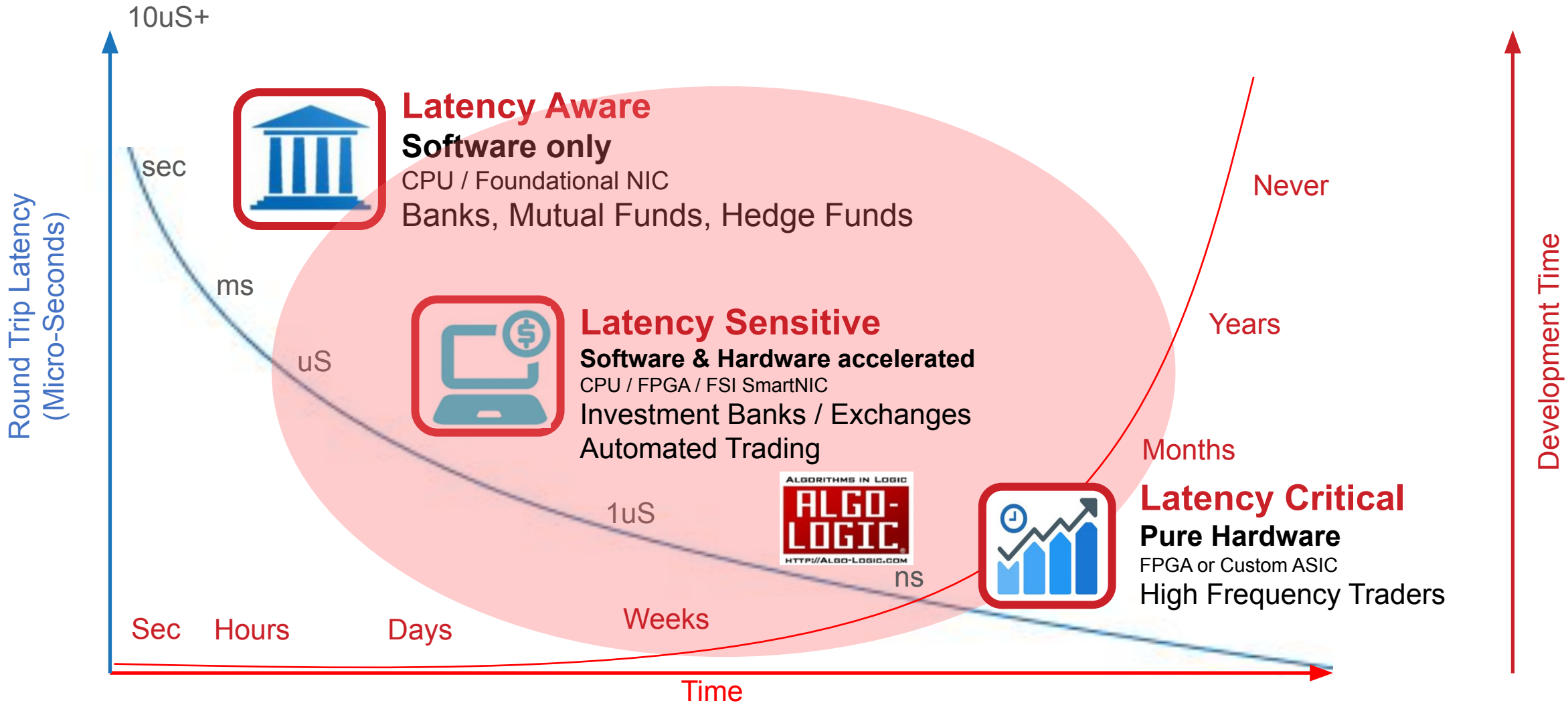
Other 3rd party NIC
- Kernel Bypass
- Default Firmware
- Low Latency Firmware

This Host+Network
- Software API
- Intel Data Mover
- Algo-Logic MAC+TCP

Algo-Logic FPGA Logic
- ULL MAC
- TCP Endpoint
- HLS Interface for trading algorithms in logic



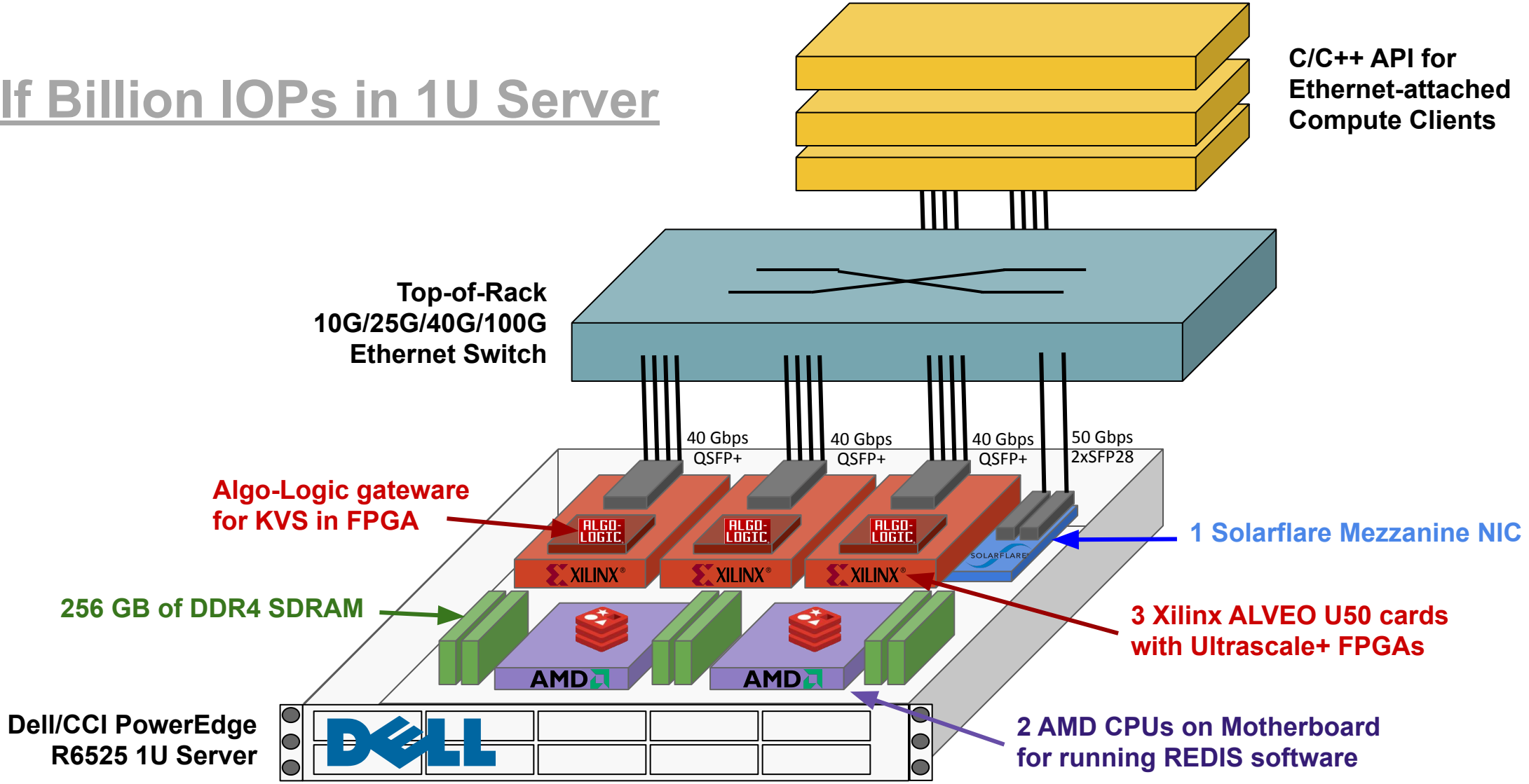
Trading Solutions: Latency vs. Development Effort



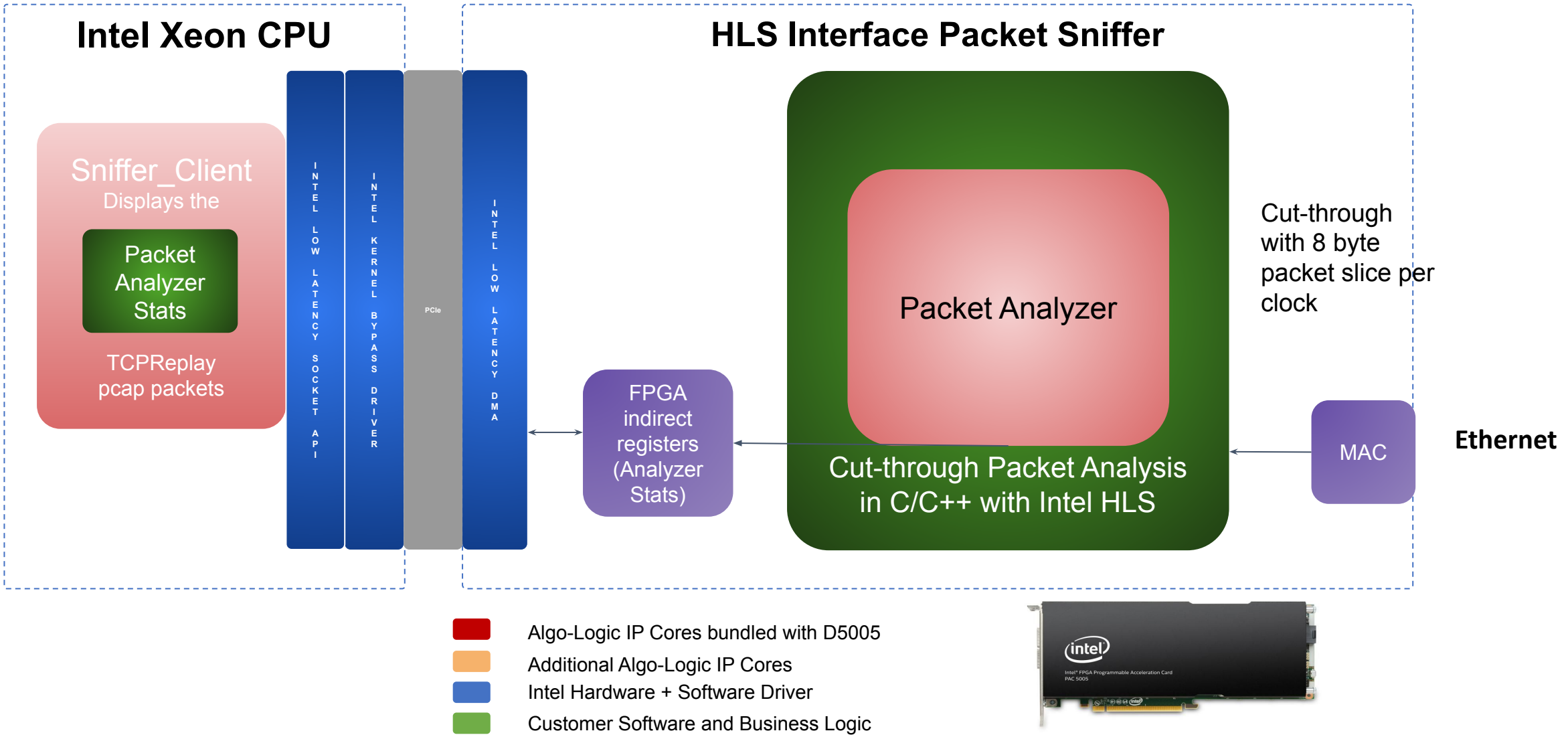
Slide from David Clarke of Intel

Algo-Logic's Key Value Store in FPGA

Half Billion IOPs in 1U Server



Algo-Logic's Cut-Through Packet Analyzer with HLS



Algo-Logic Partners & Supported FPGA Platforms

Algo-Logic provides the algorithms that run in logic on multiple FPGA platforms

Intel Programmable Acceleration Card: PAC D5005

- Stratix 10 FPGA
- On-chip SRAM
- DRAM
- 8 x 10G/25G Ethernet

Cisco Nexus SmartNIC+ V5P/V9P

- Ultrascale+ FPGA
- On+Off-chip SRAM
- DRAM
- 8 x 10G/25G Ethernet

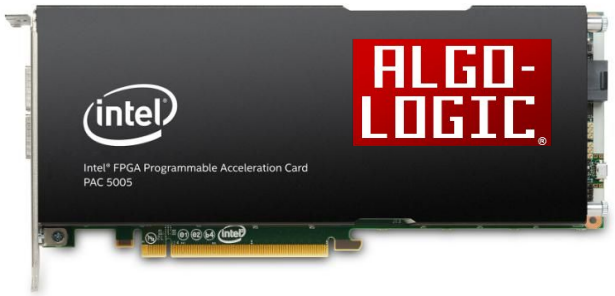
Xilinx ALVEO U50/U200/U250

- Ultrascale+ FPGA
- On-chip SRAM
- DRAM
- HBM
- 8 x 10G/25G Ethernet

Conclusion

Solution enables Ultra-Low Latency (ULL) Networking

- Leverage existing software on CPU and kernel-bypass NICs
- Migrate time-critical functions to the FPGA



Algo-Logic Products Include:

- ULL MAC, UDP, and TCP networking stacks
- Associative Lookup for Key Value Store (KVS)
- Full-stack applications running in FPGA logic
  - Trading, Database, Real-time data

Web: https://Algo-Logic.com

Twitter: @Algo_Logic_Inc

Phone: (408) 707-3740

Algo-Logic's reference platforms

- Leverage's Tool Vendor's High Level Synthesis **(HLS)** frameworks
- Off-the shelf FPGA cards from Intel, Cisco, and Xilinx
- Pre-qualified systems available for purchase directly from Dell, HPE, ...

To learn more, email us at: ***Solutions@algo-logic.com***

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Abstract

By mapping algorithms into logic, network applications can be implemented that perform full-stack processing functions with very low latency. Whereas applications written in software software typically require multiple microseconds to complete application-level functions, applications implemented in Field Programmable Gate Array (FPGA) logic process packets of data on the timescale of nanoseconds. A challenge in the past has been that the time to develop applications was typically measured in years. But today, with the help of High Level Synthesis (HLS) compilers and pre-built ultra-low-latency IP cores for networking, Algo-Logic provides complete frameworks for deploying applications for high-frequency trading, database, and other real-time applications on multiple off-the-shelf FPGA platforms from Intel, Xilinx, and Cisco.

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