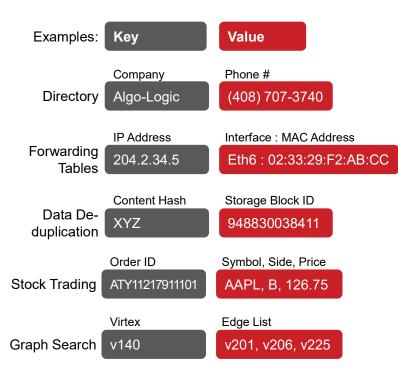
Ultra-Low Latency Key-Value Store (KVS) Gateware Defined Networking® for FPGA



Description

Key-Value Store (KVS) is an essential service for multiple applications. Telecom directories, Internet Protocol forwarding tables, and de-duplicating storage systems, for example, all need key-value tables to associate data with unique identifiers. In datacenters, high performance KVS tables allow hundreds or thousands of machines to easily share data by simply associating values with keys and allowing client machines to read and write those keys and values over standard high-speed Ethernet.



Algo-Logic's KVS leverages Gateware Defined Networking® (GDN) on Field Programmable Gate Arrays (FPGAs) to perform lookups with the lowest latency (submicrosecond), highest throughput, and least processing energy. Deploying GDN solutions save network operators time, cost, and power resulting in significantly lower Total Cost of Ownership (TCO).

Applications

- Machine Learning
- Telecom ESN and SIM key value tables
- IPv4 or IPv6 Internet addresses
- Auto-completion
- o NoSQL database acceleration
- Tuple lookups
- User preferences and profiles
- Stock market order IDs
- Inventory management
- Multiplayer game servers

Key Features

- FPGA accelerated ultra-low latency search
- Sub μ-Joule/lookup energy consumption
- Deterministic and jitter-free processing
- o 10 and 40 Gbps Ethernet line rate support
- Easy to integrate with client software via open-source multi-language APIs
- Supports standard create, read, update, and delete operations

Hardware Platforms

- Pre-programmed gateware application on a half-height or full-height expansion card that fits into a standard server
- Portable gateware supported on a range of commercially available FPGA card platforms

Software Controller API Options

 Open-source client software API compatible with C/C++, Java, Python, and other programming languages



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GDN-Search Reference Design Metrics

Key/Value Search Rate	Up to 170 MSPS (Million Searches Per Second) per FPGA card
Table Depth	From 48K entries in on-chip RAM to 12M entries per EMSE2 core with DDR SDRAM
Key Size	96 bits
Value Size	96 bits for fast table, 352 bits for large table
Latency	Sub 500 nanoseconds (~88x less latency than with sockets)
Throughput	Line-rate network interface speeds of 10GE to 40GE
Power Consumption Rate	Less than 0.52 μ-Joules/message (~21x less than with software sockets)
FPGA Devices Supported	Altera Stratix V, Arria 10, Stratix 10, Xilinx Ultrascale
Platforms Supported	Intel® PAC D5005, Cisco SmartNIC+ V5P, Xilinx Alveo U50/U200/U250

Gateware Search Block Diagram

