FPGA Accelerated Development Framework – V5P Standard or Enhanced

Algo-Logic Gateware on the Cisco Nexus SmartNIC+ V5P FPGA hardware platform

Description

Field Programmable Gate Arrays (FPGA) are being used in a wide range of applications including High Frequency Trading, Risk Compliance, and real-time data because they offer:

Flexibility – Functionality of the device can be reconfigured to match the specific requirements of the solution

Acceleration – Network response times with deterministic and deep sub-microsecond latency by processing data directly in FPGA logic

Alpha Generation – Algorithms programed in logic consistently run faster than those in software and provide an edge to trading clients

Through our partnership with Cisco, Algo-Logic is changing the way companies design and implement FPGA accelerated solutions. The result enables your team to bring new applications featuring FPGA acceleration to market quickly.

The framework solution leverages Algo-Logic's proven Ultra-Low Latency MAC and TCP Endpoint along with the Cisco Nexus Firmware Development Kit (FDK-PE) featuring an Ultra-Low Latency PCIe DMA interface and High-Level Synthesis tools. Cisco's HLS enables you to compile and synthesize business logic that runs entirely on the FPGA and interfaces directly to 10GE.

Algo-Logic's enhanced framework adds a Key Value Store (KVS) implemented with Algo-Logic's Exact Match Search Engine (EMSE) as well as a UDP/IP Engine, both implemented entirely in logic. The result is that messages in Ethernet packets can be processed directly by the FPGA. This Enhanced Framework enables building complex solutions for Tick-to-Trade (T2T), Pre-Trade Risk Checks (PTRC), and other real-time data applications.

FPGA-Accelerated Applications

- **Tick-to-Trade (T2T)**
  - Ultra-Low-Latency with deep sub-microsecond, deterministic network response times
  - Flexible – Develop triggers in RTL, HLS, or software that respond to market data in UDP/IP and send orders over TCP/IP from logic
  - Adaptable – Parse market data and generate your own orders from HLS to bring FPGA acceleration to new venues

- **Pre-Trade Risk Check (PTRC)**
  - Leverages a decade of PTRC experience by Algo-Logic to ensure your orders are verified as they are sent from your clients to the exchange.
  - Perform the checks with deep sub-microsecond latency and deterministic processing times.
  - Flexible – HLS allows developers with C/ C++ experience to implement proprietary checks

- **Real-Time Data**
  - The reference platform is ideal for all types of applications that need to process network data quickly and deterministically

Fast Time to Market

Algo-Logic's prebuilt, field proven IP Cores

- ULL 10GbE MAC+PHY (Ultra-Low-Latency Ethernet)
- ULL TCP/IP Endpoint (reliable order flow processing)
- ULL EMSE (Key Value Store for associative lookup)
- ULL UDP/IP Engine (read packet data directly to logic)

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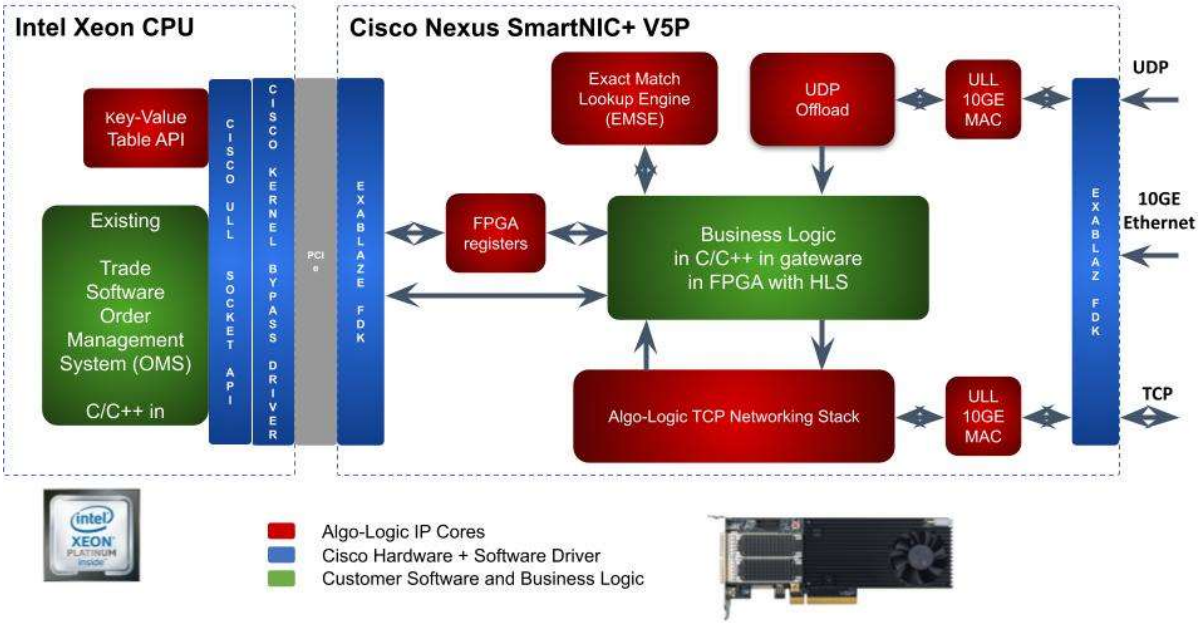
FPGA Accelerated Development Framework
Standard Framework and Enhanced Framework

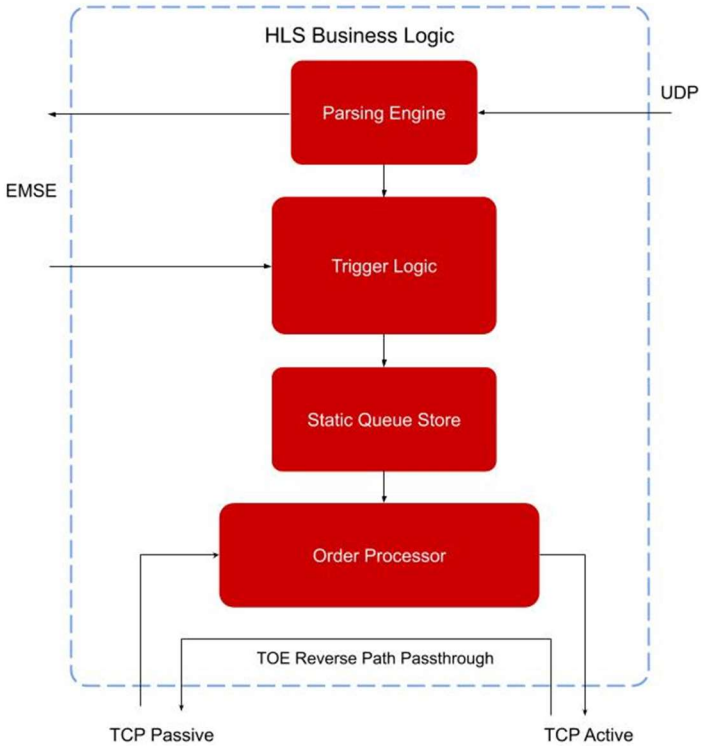
The standard framework available from Algo-Logic includes Algo-Logic's Ultra-Low Latency 10GbE MAC+PHY, TCP/IP, High Level Synthesis (HLS) Business Logic block, and the Ultra-Low Latency PCIe DMA engine to interface with software. Algo-Logic's extended framework adds a Key Value Store (KVS), UDP/IP offload to enable associative lookup, and examples of HLS C++ source code that interfaces with all the IP Cores.



The Enhanced Framework HLS business strategy block includes a region linking a Receive Only UDP instance, full stack TCP Proxy endpoint and an EMSE instance as shown.

The Framework for the Cisco Nexus SmartNIC+ V5P is designed to work with Cisco Nexus FDK-PE and Vitus development tools.

The Enhanced Framework is well suited for applications that require maximum line rate performance or ultra-low latency including: Tick-to-Trade, PreTrade Risk Checks, and other real-time data processing applications.



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