Ultra-Low-Latency Exact Match Search Engine

Description
Algo-Logic Systems’ Ultra-Low-Latency (ULL) Exact Match Search Engine (EMSE) IP is latency-optimized key-value lookup system for accelerated finance applications. Algo-Logic’s EMSE core has the unique ability to maintain constant lookup time through an advanced table balancing algorithm input instead of a variable lookup delays due common with trees and/or hash probing algorithms.

The EMSE stores a value along with each entry/key whereas a typical lookup engine requires an additional memory lookup after a match address has been found. Therefore, value is returned along with the match without an extra memory lookup, thus reducing latency.

EMSE can be used either as a stand-alone FPGA IP using the hardware command interface or with an API so that data can be shared between software and logic on FPGA.

Features and Benefits
- Supports following commands in logic and software
  - Insert (Key, Value)
  - Value = Search (Key)
  - Modify (Key, Value)
  - Delete (Key)
- Parameterizable field and table sizes
  - Key sizes between 80 to 640 bits
  - Value sizes in increments of 8 bits
  - Number of entries
- Support for larger on-chip tables
  - Large tables can be stored using UltraRAM in Xilinx UltraScale+ device family
- Sharing data between logic and software
  - Hardware interface enables issuing commands from FPGA logic
  - C++ software API enables issuing commands from software
- Core tracks usage statistics

Applications
- High Frequency Trading
- Tick-To-Trade systems
- Pre-Trade Risk Check systems
- Position and Exposure tracking
Ultra-Low-Latency
Exact Match Search Engine

EMSE Metrics

<table>
<thead>
<tr>
<th>Key Size</th>
<th>80/96/128/160/320/640-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value Size</td>
<td>User configurable in increments of 8bits</td>
</tr>
<tr>
<td>Number of Entries</td>
<td>(2^n) *1024, n=1,2,… (subject to on-chip resources)</td>
</tr>
<tr>
<td>Ultra-Low Lookup Latency</td>
<td>6 clock cycles on Virtex UltraScale+*</td>
</tr>
<tr>
<td>Logic Footprint</td>
<td>8% ALMs in Stratix 10 SX2800**, ~2% CLB LUTs in XCU200 UltraScale+ on Xilinx Alveo U200**</td>
</tr>
<tr>
<td>On-chip Memory Footprint</td>
<td>19% M20K in Stratix 10 SX 2800**, 20% URAM in XCU200 UltraScale+ on Xilinx Alveo U200**</td>
</tr>
<tr>
<td>FPGA Devices Supported</td>
<td>Intel Stratix V, Intel Stratix 10, Xilinx Virtex Ultrascale+</td>
</tr>
</tbody>
</table>

* Subject to EMSE configuration and target FPGA device
**EMSE configuration: 128 bits Key, 512 bits Value, 65,536 (64K, n=6) entries

Examples of EMSE Use Cases

Symbol Parameter Table

Order State Table