Low Latency Library

Pre-built FPGA Logic for HFT Applications

Description

Algo-Logic Systems' pre-built Low Latency Library consists of infrastructure components and protocol parsers that enable processing orders with the lowest theoretical latency possible. The library is developed as a set of modular components that can be integrated together to implement a complete Algorithmic Trading Solution with the shortest possible time to market.

Infrastructure components in the library form the base of Algo-Logic's low latency finance solutions. It consists of functions such as Internet Protocol (IP) decoding, TCP session processing, UDP datagram processing, and a register interface that allows the hardware to be easily controlled from a software API. Infrastructure components for standard FPGA platforms (like the DE5Net) allow the gateware to operate on orders at full 10 Gbps line rate.

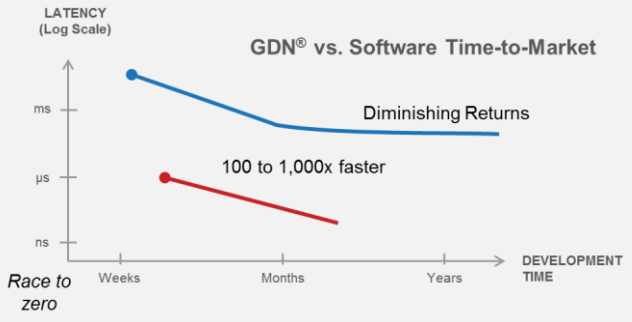
For order entry, the protocol parser library supports FIX and binary financial protocols including OUCH for NASDAQ, XPRS for DirectEdge, BOE for BATS BZX, ArcaDirect for NYSE ARCA, Arrowhead for TSE, and Native Trading Gateway for LSE. For market data parsing, we support CME MDP3 for SBE. The protocol parsers combined with business logic can extract and process data in under 0.2 µS.

Applications

- Order processing
- Risk management
- Compliance
- Trading strategy
- Internalization
- Smart order routing

Key Benefits

- FPGA gateware provides lower latency processing than can be achieved in software
  - Order data can be extracted and processed in under 0.2 µS
  - Hardware provides deterministic, jitter-free processing of messages
- By using Algo-Logic's pre-built low latency library, products can be completed without a long development time
  - The parsing libraries already support all major stock exchange protocols
  - The FPGA hardware enables highly flexible and customizable trading solutions



8=FIX.4.2 | 9=178 | 35=8 | 49=PHLX | 56=PERS | 52=20071123-05:30:00.000 | 11=ATOMNOCCC9990900 | 20=3 | 150=E | 39=E | 55=XLNX | 167=CS | 54=1 | 38=15 | 40=2 | 44=15 | 58=PHLX EQUITY TESTING | 59=0 | 47=C | 32=0 | 31=0 | 151=15 | 14=0 | 6=0 | 10=128 |

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Algo-Logic Infrastructure

Order Sessions

Supports reliable communication sessions to send stock market orders and receive execution reports.

TCP Endpoint

The full-duplex TCP/IP endpoint terminates up to 64 TCP sessions directly to FPGA logic. Sessions can be opened, maintained, and closed and data can be modified as it streams between ports.

IP Processing

The IP processing block identifies network sessions, verifies and computes packet checksums, and can perform Network Address Translation when needed.

Financial Protocol Parser

Extract data from FIX, OUCH, ARCA, ArcaDirect, XPRS, LSE, and other native market protocols.

Control

Standard C, C++, Java, or other APIs on a host computer or a web-based Graphical User Interface (GUI) can be used to control the hardware.

Logging

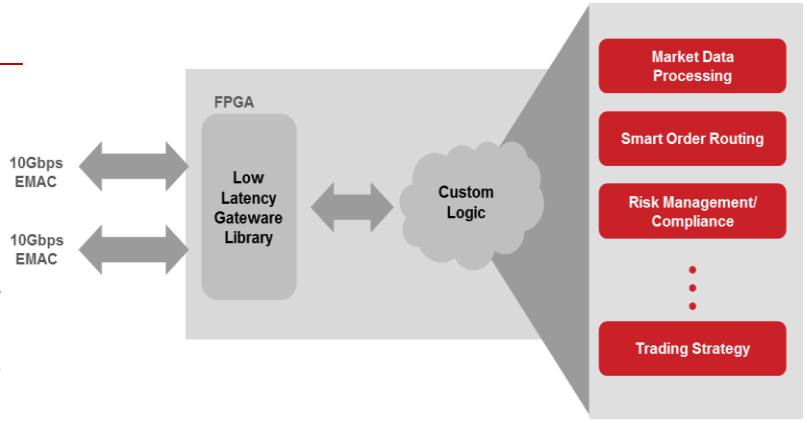
The logging module sends reports and can trigger SNMP Traps, interface with system software, and/or display events on a GUI.

Register Interface

The registers interface contains configuration, status and general purpose read/write registers. The UDP-based interface allows the FPGA to be controlled and monitored from any host on the local network.

Application Layer Logic

Custom trading algorithms implemented inside the FPGA can inject orders immediately after a market data trigger. Algo-Logic provides turn-key solutions to implement complete tick-to-trade systems.



Market Data Filter

Algo-Logic's Market Data Filter solves the problem of CPU overload during micro-bursts and peak market activity. The MDF parses, extracts, and filters market data at the full 10 Gbps line speed.

Full Order-Book

Track bid/ask prices for dozens of symbols with the lowest latency possible. The order-book maintains full L3 data and outputs L2 books with a programmable depths and intervals.

Stock Price Table

Prices for thousands of symbols can be stored in memory and updated from the order-book using on-chip memory or in off-chip SRAM.

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